IN THE SPECIFICATION

On page 1, please amend the title "BACKGROUND OF THE INVENTION" by removing the underlining as follows:

BACKGROUND OF THE INVENTION

On page 1, please amend the title "Field of the Invention" by removing the underlining as follows:

Field of the Invention

On page 1, please amend the title "Description of the Related Art" by removing the underlining as follows:

Description of the Related Art

On page 1, please amend the title "BRIEF DESCRIPTION OF THE DRAWINGS" by removing the underlining as follows:

BRIEF DESCRIPTION OF THE DRAWINGS

On page 2, please amend the title "DETAILED DESCRIPTION OF THE INVENTION" by removing the underlining as follows:

DETAILED DESCRIPTION OF THE INVENTION

On page 19 listing the "ABSTRACT OF THE DISCLOSURE," please amend the title by removing the underlining as follows:

ABSTRACT OF THE DISCLOSURE

On page 2, after paragraph [0010], please add the following two new paragraphs:

Figure 8 illustrates a register file buffer.

Figure 9 illustrates a block diagram of a process of an embodiment.

Please amend paragraph [0014] as follows:

In one embodiment of the invention, register file buffer 130 comprises ~~an~~ integer register buffer 810 and ~~a~~ predicate register file buffer 820 (illustrated in **Figure 8**). In one embodiment of the invention ~~the~~ integer register file buffer 810 comprises a plurality of write ports, a plurality of checkpoints and at least one read port. ~~The~~ iInteger register file buffer 810 is used to communicate register values from commit processor 110 to speculative processor 120. In one embodiment of the invention, ~~the~~ integer register file buffer 810 comprises eight (8) write ports, four (4) checkpoints, and one (1) read port to access any of the checkpointed contexts. In one embodiment of the invention, ~~the~~ integer register file buffer 810 has an eight (8) register wide array and sixteen (16) rows. In one embodiment of the invention, ~~the~~ predicate register file buffer 820 comprises a plurality of write ports, a plurality of checkpoints and at least one read port. ~~The p~~ Predicate register file buffer 820 is used to communicate register values from commit processor 110 to speculative processor 120.and a second level register file coupled to speculative processor 120. In one embodiment of the invention, ~~the~~ predicate register file buffer 820 comprises eight (8) write ports, four (4) checkpoints, and one (1) read port to access any of the checkpointed contexts. In one embodiment of the invention, ~~the~~ predicate register file buffer 820 has an eight (8) register wide array and eight (8) rows.

Please amend paragraph [0029] as follows:

In one embodiment of the invention the store ID and/or load ID 550 is an index into an entry in trace buffer 140, which is unique per instruction. In one embodiment of the invention the store valid bit is set to zero ("0") if a load hits store buffer 160. In this embodiment of the invention, the store valid bit is set to one ("1") if the load missed store buffer 160. In one embodiment of the invention, a replayed store that has a matching store ID clears (sets to "0") the store valid bit and sets the mispredicted bit in the load entry in trace buffer 140. In one embodiment of the invention, a later store in the program that matches tag portion 520 clears (sets to "0") the store valid bit and sets the mispredicted bit in the load entry in trace buffer 140. In one embodiment of the

invention, a clean (not replayed) store that matches the store ID sets the store valid bit to "1" (one). In one embodiment of the invention, upon a clean (not replayed) load not matching any tag portion 520, or a load matching tag portion 520 with the store valid bit clear (set to "0"), the pipeline is flushed, the mispredicted bit in the load entry in trace buffer 140 is set to one ("1"), and the load instruction is restarted. In one embodiment of the invention, when a load entry is retired, entry valid bit portion 530 is cleared. Figure 9 illustrates a block diagram of a process including setting/clearing the above status bits, and instruction pipeline flow.

IN THE TITLE

Please replace the title of the invention with the following new title:

A METHOD, APPARATUS AND SYSTEM FOR MULTI-THREADED EXECUTION OF A SINGLE THREAD ON MULTIPLE PROCESSORS WHERE ONE PROCESSOR SPECULATIVELY EXECUTES THE SINGLE THREAD AHEAD OF ANOTHER PROCESSOR AND SHARES CONTROL INFORMATION COMMITMENT OF RESULTS